REMARKS

Claims 1-3 and 20-36 are pending in the application.

No Claims have been amended, and reconsideration is respectfully requested.

Applicant incorporates by reference its remarks made in Applicant's Amendment and Response to Final Office Action faxed to the United States Patent and Trademark Office on July 30, 2007. Attached are the three (3) pages, as requested by the Examiner.

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@munckbutrus.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Munck Butrus Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS CARTER, P.C.

Date: Nov 29, 2007

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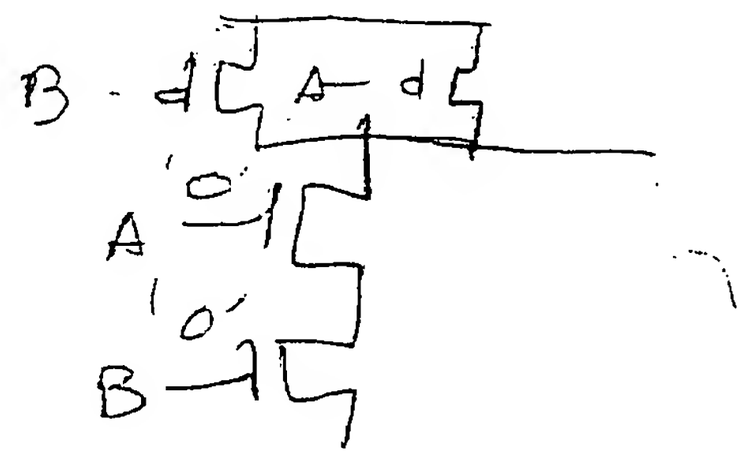
Recently it has been proposed [a] that certain input vector combination can be applied to circuits in order to reduce the total leakage current that the design expends. For example for a 2-input NAND gate, it may be more advantageous to provide an input vector of 00 to reduce leakage power over other input combinations. This problem is further complicated by gate leakage [not discussed in [1]]. To illustrate the issue see the figure below



The technique of Boolean satisfiability can be used to determine the ~~lowest~~ set of input value that will minimize total leakage current [1].

The issue then arises as to how a low leakage vector set should be applied. A simple solution

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Date [redacted]

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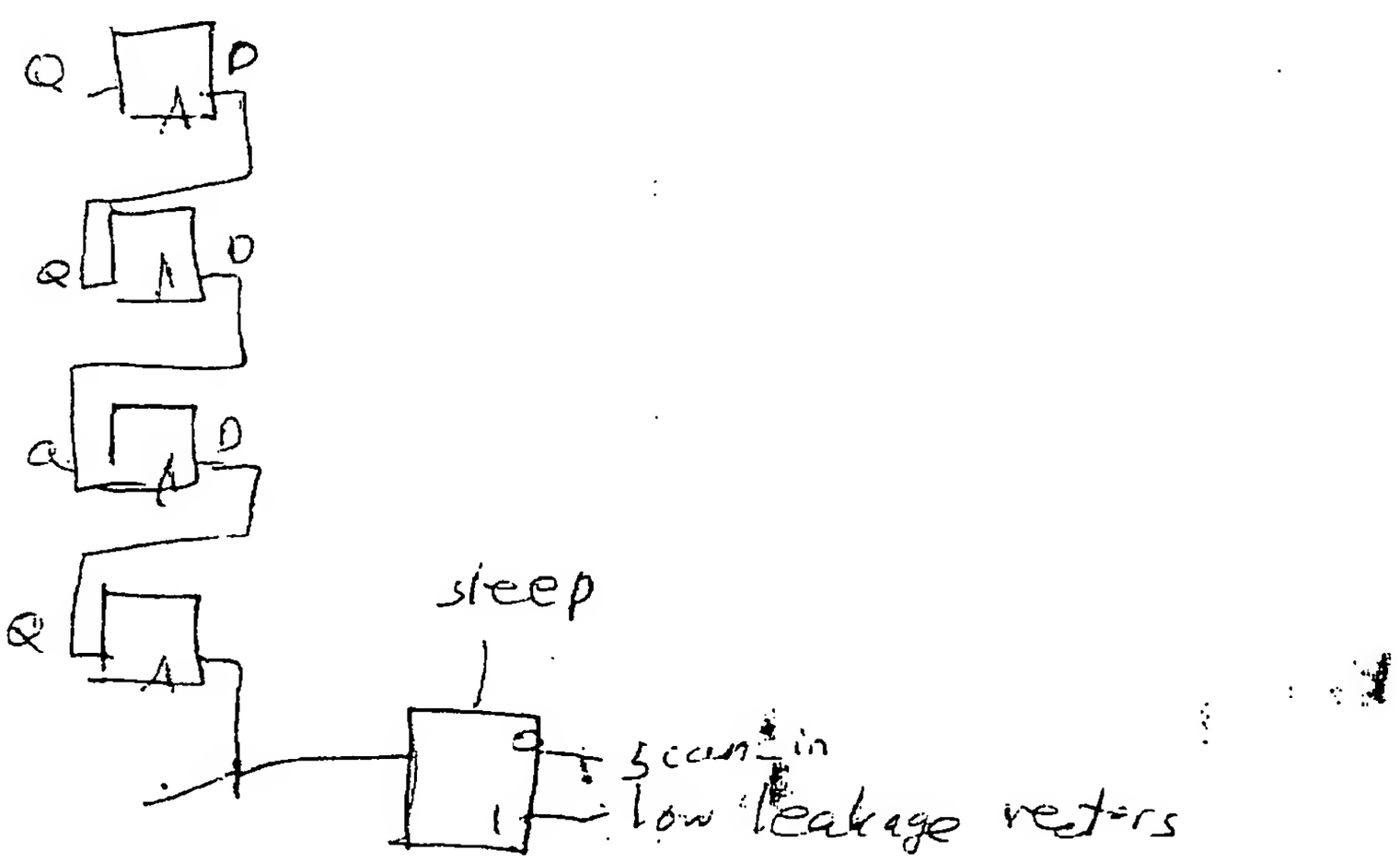
Recorded by Razak Hossain

Date [redacted]

(and elegant) one is to use a scan chain to insert the low leakage state when the design is in sleep mode. This can be done with only one extra input signal to the design. Let us call this signal "sleep." The input signals can be generated on-chip from a BIST or provided from off-chip via the scan in port. A mechanism to ensure that only the right number of input scan vectors are provided can be done by an FSM based counter or some other mechanism.



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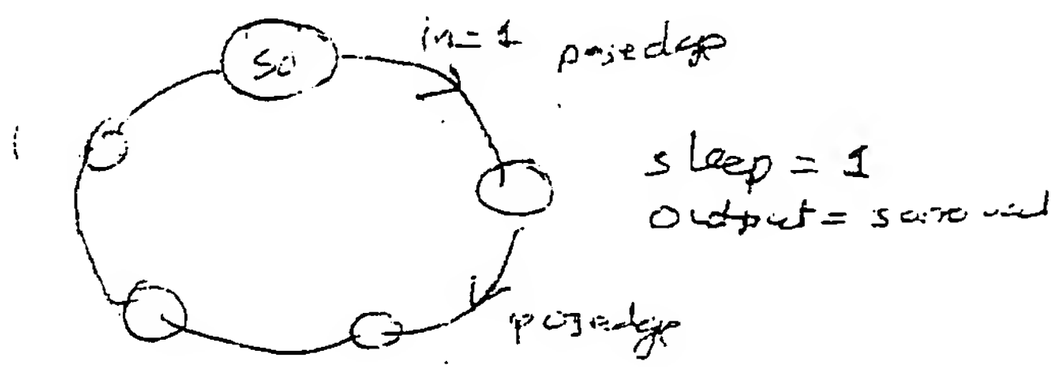
The sleep signal be an internal or external signal.

FSM counter



This approach has advantages over that proposed in [2] because only 2 external ports are needed for initiating it (provided an external "sleep" and sleep scan en" signal are provided, Also, since the scan chain is used to supply the input vector there are 2 other advantages with it:

① There is no extra delay overhead, and,
② No extra routing of data signals to individual flip-flops is required.

[1] F.A. Aloul, S. Hassoun, K.A. Sakallah, D. Blaauw "Robust SAT-Based Search Algorithm for Leakage Power Reduction" International Workshop on Power and Timing Modeling Optimization and Simulation (PATMOS), Seville Spain 2002.

[2] A Chandrakasan, W. Bowhill, F. Fox eds, "Design of High-Performance Microprocessor Circuits," Piscataway NJ IEEE Press, 2001

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